Nithin Chatterji

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Research Interests

Modeling of silicon based carrier selective solar cells, Perovskite solar cells, gated solar cells for dynamic recovery of efficiency. Device simulation and modelling, Semiconductor device physics, Photoelectrochemical water splitting.

Education

Indian Institute of Technology Bombay, Mumbai, India

M. Tech + Ph.D Dual degree, Electrical Engineering, July 2012 - May 2019

- **Thesis Topic**: *Modeling of Interface Dependent Efficiency and Temperature Coefficient of Silicon Based Carrier Selective Solar Cells*
- **Submitted**: Feb 2019
- **Defended**: May 2019
- **Supervisor**: Prof. Pradeep R. Nair

University of Kerala, Thiruvananthapuram, India

B.Tech, Sree Chitra Thirunal College of Engineering, Thiruvananthapuram, Electronics and Communication Engineering, October 2004-May 2008

Professional Experience

Sardar Vallabhbhai National Institute of Technology Surat
Department of Electronics Engineering
Assistant Professor April 2021 to present

Indian Institute of Technology Bombay
Department of Electrical Engineering
Research Associate February 2019 to August 2019
Project Research Associate September 2019 to March 2021

Supervisor: Prof. Pradeep R. Nair

- Self doping effects in Perovskite solar cells
- Optimum architecture for silicon based carrier selective solar cells
- Novel architecture for dynamic recovery of efficiency

Accenture Services Pvt. Ltd.
Software Engineer August 2008 to April 2011

Refereed International Journal Publications

Published

1. **N. Chatterji** , S. Bhatia, A. Kumar, A. Antony, and P. R. Nair , "Material and Process Tolerant High Efficiency Solar Cells with Dynamic Recovery of Performance", *IEEE Transactions on Electron Devices . (Impact factor: 2.970)*, vol. 68, no. 4, pp. 1676-1681, April 2021, DOI: 10.1109/TED.2021.3056954.

2. **N. Chatterji** , and P. R. Nair , "Electron vs. hole extraction: Self doping induced performance bottleneck in Perovskite solar cells", *IEEE Electron Device Letters (Impact factor: 4.020)*, vol. 40, no. 11, pp. 1784-1787, Nov. 2019, DOI: 10.1109/LED.2019.2944474.

3. **N. Chatterji** , A. Antony, and P. R. Nair , "Temperature coefficient of Silicon based carrier selective solar cells", *IEEE Journal of Photovoltaics (Impact factor: 3.890)*, vol. 9, no. 3, pp. 583-590, May 2019, DOI: 10.1109/JPHOTOV.2019.2892127.

4. **N. Chatterji** , A. Antony, and P. R. Nair , "Interface-Dependent Efficiency Tradeoff in Si-Based Carrier-Selective Solar Cells", *IEEE Transactions on Electron Devices (Impact factor: 2.970)*, vol. 65, no. 6, pp. 2509–2516, Jun. 2018, DOI: 10.1109/TED.2018.2822938.

Under Preparation

1. **N. Chatterji**, and P. R. Nair , "Optimal Device Architecture for Si based Carrier Selective Solar Cells".
2. N. R. V. Satish, V. Garg, and **N. Chatterji** , "Perovskite-inspired Cu2AgBiI6 solar cells for indoor photovoltaics".
3. **N. Chatterji**, and P. R. Nair , "Quasi static analysis of trapping dominated PL response".

Conference Publications

Published

1. S. Manjhi, **N. Chatterji**, B. S. Sengar, and V. Garg, "Optimization of BiOI/HTL Heterojunction for Efficient Charge Extraction from Solar Cell: For Indoor Light Harvesting, ", *40th European Photovoltaic Solar Energy Conference (EuPVSEC 2023)*, Lisbon, Portugal, September 2023.
2. **N. Chatterji**, and P. R. Nair, "Minimum bandgap criteria for carrier selective layers in Si solar cells, ", *40th European Photovoltaic Solar Energy Conference (EuPVSEC 2023)*, Lisbon, Portugal, September 2023.
3. Anil Kumar, **N. Chatterji**, A. Antony, and P. R. Nair,"Influence Of Bulk Carrier Lifetime On Efficiency Recovery In Gated Solar Cells", *8th World Conference on Photovoltaic Energy Conversion (WCPEC-8)*, Milan, Italy, September 2022.
4. **N. Chatterji**, A. Antony, and P. R. Nair, "Interface quality: Effect on performance of Silicon based Carrier Selective solar cells", *2019 AIP 3rd International Conference on Optoelectronic and Nano Materials for Advanced Technology (ICONMAT 2019)*, Kochi, India, January 2019.
5. **N. Chatterji**, A. Antony, and P. R. Nair, ''Effect of bulk doping in Si based carrier selective solar cells", *2018 IEEE 4th International Conference on Emerging Electronics (ICEE 2018)*, Bangalore, India, December 2018.
6. Anil Kumar, Shaurya Arya, **N. Chatterji**, A. Antony, and P. R. Nair, ''Rear Contact Dependent Performance Enhancement of PEDOT:PSS/n-Si Solar Cell", *2018 IEEE 4th International Conference on Emerging Electronics (ICEE 2018)*, Bangalore, India, December 2018.
7. I. M. Khorakiwala, K. K. Markose., A. Kumar, **N. Chatterji**, P. R. Nair, and A. Antony, ''Studies on n-Type a-Si:H and the Influence of ITO Deposition Process on Silicon Heterojunction Solar Cells", *2017 19th International Workshop on Physics of Semiconductor Devices (IWPSD 2017)*, New Delhi, India, December 2017.
8. **N. Chatterji**, S. Khatavkar, C. Voz, A. Morales-Vilches, J. Puigdollers, B. M. Arora, A. Aldrin, and P. R. Nair, ''A Critical Analysis on the Role of Back Surface Passivation for a-Si/c-Si Heterojunction Solar Cells", *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC 2014)*, Denver, Colorado, US, June 2014.

Honors and Awards

- Award for Excellence in Ph. D. research (2017-2019) IIT Bombay.
- Best poster award at ICONMAT 2019.
- Best poster award at ICEE 2018.
- Qualified GATE 2012 with a rank 113 and a 99.93 percentile.

Projects

- Dr. Vivek Garg, Dr. Deepak Joshi, **Dr. Nithin Chatterji** and Dr. Abhishek Acharya, 'Design and Fabrication of BiOI based Indoor Photovoltaic Devices for Development of Self-Powered IOT Ecosystem', Budjet- Rs. 11 Lakhs, funded by i-Hub Divyasampark.

Expert Talks

- Lecture on ''DRAM'' in FDP organized by NIT Warangal on ''Introduction to Low power VLSI design and Applications''.
- Lecture on ''Introduction to DRAM'' in FDP organized by NIT Warangal on ''LOW POWER VLSI DESIGN''.

Labs Developed

- Semiconductor Manufacturing & Testing Center (SMTC)
- Semiconductor Technology (SemTecc) Laboratory
- Design and Simulation (DeSim) Laboratory

Teaching Experience

Department of Electronics Engineering — Autumn 2021 - Present
Sardar Vallabhbhai National Institute of Technology, Surat

EC 622: Low Power VLSI Design	Spring 2024
EC 106: Digital Electronics and Logic Design	Spring 2024
EC 403: Fundamental of Nanoelectronics	Autumn 2023
EC 638: VLSI System Design	Spring 2023
EC 622: Low Power VLSI Design	Spring 2023
EC 203: Digital Logic Design	Autumn 2022
EC 408: VLSI System Design	Spring 2022
EC 211: Electronic Circuits	Autumn 2021

Teaching Assistant — Autumn 2012 - Autumn 2016
Department of Electrical Engineering
Indian Institute of Technology Bombay

EE735: Microelectronics Simulations Lab	Autumn 2016, 2015
EE344: Electronic Design Lab	Spring 2016
EE112: Introduction To Electronics	Spring 2015
EE236: Electronic Devices Lab	Autumn 2014
EE209: Electrical/Electronics Lab	Spring 2014
EE214: Digital Circuits Lab	Spring 2013
EE337: Microprocessor Lab	Autumn 2012, 2013

National and International level professional engagements/ contributions

- Collaborated with a team from Universitat Politècnica de Catalunya headed by Dr. Cristabol Voz, which resulted in one conference publication.
- Involved in the modelling of c-Si/a-Si heterojunction solar cells with Solar Energy Research Institute for India and the United States (SERIIUS) form Jan- 2013 to Feb-2017.
- modelling of silicon based carrier selective solar cells with National Center for Photovoltaic Research and Education (NCPRE) at IITB from Feb-2017 to Present.

References

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Indian Institute of Technology Bombay

Prof. Anil Kottantharayil
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Associate Professor
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Cochin University of Science and Technology
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