RESUME

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1. Personal profile:

Name	:	ZUBER M. PATEL
Date of birth	:	02-09-1975
Father's name	:	Mahmood A. PATEL
Languages known	:	English, Hindi, Gujarati
Nationality	:	Indian
Permanent address	:	201, Evergreen Complex – B Wing, Morabhagal, Rander Road, Surat – 395005. Gujarat. INDIA mobile: +919898698793

2. Education:

Course	Year	Institution	Grade
12TH Std. (Science)	1993	Gujarat Board, Gujarat	Distinction
B.E. Electronics	1998	NIT Surat, (formerly REC) Gujarat. India	Distinction
M. Tech (Microelectronics and VLSI)	2009	I I T, Bombay, India	9.29 /10 CGPA
PhD	2018	NIT Surat. Gujarat. India	N.A.

- **M.Tech Dissertation** was based VLSI (FPGA & ASIC) implementation of baseband processor for broadband wireless system (interleaving, error correcting codec, mapping etc.)
- **PhD work** was based on Design, Development and Implementation of Novel Packet Scheduling Algorithms for wireless broadband network for uplink and downlink transmissions.

3. TOTAL EXPERIENCE: (Total 27 years 2 months) as on Aug. 2026

(Teaching: 25 Years, Industry: 2.3 Years)

- **Present Employment:** (**24** years)

Associate Professor, Electronics Engg**.** Dept., **S.V. National Institute of Technology (SVNIT)**, Surat, India. (www.svnit.ac.in)

- Teaching in Electronics & Communication engineering courses
- Guiding and Handling the UG and PG projects/dissertations
- Managing laboratories as a Laboratory In charge
- Perform instructionally related duties such as curriculum development, program outcomes assessment, student advising and mentoring.
- Engage in research projects and development

- **Previous Employment 1:** (**11** months)

Faculty, Electronics Engg. Dept., Nirma Institute of Diploma Studies, Ahmedabad, India, Sept. 2001 to Aug. 2002

- Teaching in Electronics engineering subjects
- Allied works related to academics and administration

- **Previous Employment 2:** (**2** years **3** Months)

System and Network Administrator, CMS Computers, Surat.
Dec.1998 – Mar. 2001

- Computer hardware, networking and administration using Network OS.
- Windows Servers and Workstations management
- LAN/WAN installation with switches, hubs and bridges.

4. PUBLICATIONS:

- **13** International Journal and **17** International Conference Publications (Appendix – A)

5. RESEARCH WORK:

- **Co-coordinator** of **Research Project** named VLSI SMDP-II from MCIT, Govt. of India. The research project was related to VLSI Design and for the duration of **5 years (2006-2011** extended up to Mar. 2013**).**
- Member of Investigators of **C2SD Research Project (**Duration: **5 years** i.e. **2016 to 2021)**

from MeitY, Govt. of India. In this project, I am involved in ASIC design for Error-Correcting Codec for low power high speed serial transceiver for space application.

- Co-Principal Investigators of **C2S (Chip to Startup) Research Project (**Duration: **5 years** i.e. **2024 to 2028)** from MeitY, Govt. of India. In this project, I am involved in design of "Digital in Memory computing ASIC" and other Emerging Technologies for in memory computing.
- **Supervising PhD Students**: 3 PhD completed, 3 ongoing
- **M.Tech Dissertation**: 15 Dissertation in last 5 years (50 in total)

6. Research Interests:

- Digital VLSI Design and Embedded Systems
- RISC Micro-processors architectures and SoC
- Digital Baseband system of Wireless transceiver

7. SKILLS:

- Assembly and embedded C programming for embedded system
- HDL/FPGA based design with ModelSim and Vivado Suit
- Cadence/Synopsis tool set related to ASIC design
- Linux/Windows OS, C/C++ programming

APPENDIX – A Publications:

Total Publications= 15 (Int. Journals) + 17 (Int. conf.) = **32**

International Journals:

[1] Kinnar G. Vaghela and Z.M.Patel; "Optimizing performance of Spectrum Subtraction using the Time Frequency Filtering"; International Journal of Research and Reviews in Electrical and Computer Engineering (IJRRECE) ; Vol. 1, No. 2; Science Academy Publisher, UK. ISSN: 2046-5149; **Mar. 2011**

[2] Nilesh Ranpura, Prof. Z.M.Patel and Ekta Mehul; "Simulation of unified architecture of IEEE 802.11a and 802.16a PHY layers using MATLAB" ; International Journal of Computer Science & Emerging Technologies ; Vo.2, No.2 ; ISSN: 2044-6004 ; **April 2011**

[3] Kinnar vaghela and Prof. Z.M.Patel ; "Optimized Technique for Speech Noise Elimination using Traditional Spectrum Subtraction" ; IUP Journal of Telecommunication ; Vol.3, No.2 ; ISSN: 0975-5551 ; **May 2011**

[4] Jignesh Oza, Z.M.Patel, Upena Dalal & et. al. ; "Optimized configurable OFDM design blocks for Wi-Fi and Wi-Max" ; International Journal of Research and Reviews in Electrical and Computer Engineering (IJRRECE) ; Vol.1, No.3 ; Science Academy Publisher, UK. ISSN: 2046-5149 ; **Sept. 2011**

[5]. Z.M.Patel and U.D.Dalal, ―Design and Implementation of Low Latency Weighted Round Robin (LL-WRR) Scheduling for High Speed Networks,‖ International Journal of Wireless and Mobile Networks (IJWMN) AIRCC Pub., vol. 4, no. 6, **Aug. 2014**

[6]. Z.M.Patel and U.D.Dalal, "Enhancing Performance of Internetworking with Novel RED-AT Congestion Control Algorithm," International Journal of Scientific and Engineering Research (IJSER) Pub., vol.5, no. 11, **Nov. 2014.**

[7]. Z.M.Patel and U.D.Dalal, "Implementation and Evaluation of Dynamically Weighted Low Complexity Fair Queuing (DWLC-FQ) Algorithm for Packet Scheduling in WiMAX Networks," International Journal of China Communications (SCI Journal-Cosponsored by IEEE ComSoc and CIC**),** Accepted: 14 Sept. 2015, Published: **May 2016**

[8] Z.M.Patel, "Low Noise and Low Distortion Telescopic OTA for Biomedical Signal Processing", Journal of Recent Advances in Electrical & Electronic Engineering, Bentham Science Publishing ; Vol.12, No.1 ; Bentham Science Publishing, UK. ISSN: 2352-0973; Accepted: 2nd July, 2018, Published: **Dec. 2018**

[9] Navin Kabra and Z. M. Patel, "Novel Approach to Design Hard Multiple Generator for Radix-8 Modulo 2n-1 Multiplier using Inclusive-OR Adder", Integration, the VLSI Journal, Elsevier (SCI), ISSN: 0167-9260, Published: **25 July, 2020**

[10] Navin Kabra and Z. M. Patel, "Radix-8 Modulo 2n Multiplier Using Area and Power Optimized Hard Multiple Generator", Computers and Digital Techniques. IET (SCI), ISSN: 1751-861X, Published: **13 Dec., 2020**

[11] Deergha Agarwal, Zuber Patel and K. Inamdar, "Area Efficient and Linear MMIC Based Ka Band Power Amplifier for 5G Communication Systems", Journal of Integrated Circuits and Systems, (Scopus) SDMicro & SBC. ISSN: 1872-0234, Vol. 18, No. 3, Accepted: **16 oct., ,2023**

[12] Prajakta More and Zuber Patel, "Throughput and BER Analysis in LoRa Technology for Performance Enhancements using Dynamic Measurement", Journal of Wireless and Mobile Computing (Scopus). Inderscience, ISSN:1741-1092, Vol. 26, No. 4, Accepted: **14 Jan. 2024**

[13] Prajakta More and Zuber Patel, "Low power decentralized differentially private multi-armed bandit algorithm based performance improvement on long-range radio network", Journal of Wireless Networks (SCI). Springer. Vol. 30, **Accepted: July, 2024**

[14] Deergha Agarwal, Zuber Patel and K. Inamdar, "Wideband GaN HEMT Doherty Power Amplifier for 5G and Satellite Applications", International Journal Of Electronics (SCIe), ISSN: 0020-7217, Accepted: **Jan.,2026**

[15] Deergha Agarwal, Zuber Patel and K. Inamdar, "A high gain 3-stage LNA using band pass filter based matching network for 5G applications", International Journal of Information Technology, ISSN: 2511-2104, **Accepted: Mar.,2026**

International Conferences:

[1] Jignesh Oza, Z.M. Patel, Nilesh Ranpura & et. al. ; "Optimized Configurable Architecture of Modulation Techniques for SDR applications." ; International Conference on Coumputer & Communication Engg. (ICCCE'10) ; ISBN: 978-1-4244-6235-3 ; pp. 494-498 ; IEEE ; **May 2010.**

[2] Devashish Raval, Z.M. PateL,Nilesh Ranpura and Ekata Mehul ; "Comparative Analysis of OFDM parameters in WiFi and WiMAX Technologies" ; International Conference on Signals, Systems and Automation (ICSSA 2011) ; GCET, **Jan. 2011**

[3] Z.M.Patel and U.D.Dalal, "Implementation and Analysis of Downlink scheduling for

802.16 networks using Controlled Priority Queuing (CPQ)," in proceeding of SPRINGER International Conf. on Advanced Computing (ICAdC 2012), vol.174, pp.399-406, **July 2012.**

[4] Z.M.Patel and U.D.Dalal, "Performance Evaluation and Comparison of Queue Scheduling Schemes for WiMAX under Heterogeneous Traffic," in proceedings of IEEE International Conf. Circuits, Controls and Communication (C3 2013)**,** paper ID:100, **Dec. 2013.**

[5] Z.M.Patel, "Power and Area Efficient Hardware Architecture for WiMAX Interleaving"; International Conference on Communication and Signal Processing, ICCSP 2014, Bangkok ; paper ID: SP0020 ; IACSIT ; **Oct. 2014**

[6]. Z.M.Patel and U.D.Dalal, "Improved CAC Scheme for WiMAX with Adaptive Bandwidth Reservation and Degradation Policy," in proceedings of International Conferenc**e** on Computer, Electrical & Electronics Engineering (CEEE'15), Phuket, Thailand. paper ID:100, 3-4 **Oct. 2015**

[7] Z.M.Patel, "Enhancing Speed and Reducing Power of Shift and Add Multiplier', International Conference on Communication and Signal Processing (ICCSP), Thailand,

Publisher: Research World, ISBN: 978-93-85973-31-4, 12-13th **April, 2016**

[8] J.R.Prajapati and Zuber M. Patel, "High linearity low noise figure mixer for Wi-max in 0.18 μm tsmc technology", In Proc. of IEEE Conference on "Signal and Information Processing (IConSIP)", DOI: 10.1109/ICONSIP.2016.7857456, **Oct. 2016**

[9] Z.M.Patel, “Queue occupancy estimation technique for Adaptive threshold based RED”, IEEE conf. on ICCS, , pp. 437-440, DOI: 10.1109/ICCS1.2017.8326038, **Dec. 2017**

[10] Z.M.Patel, “Configuratble Mapper and Demapper for Physical Layer of SDR based wireless transceiver”, Springer ICCCPE 2018, DOI:10.1007/978-981-13-0212-1, **Jan. 2018**

[11] Z.M.Patel, “Modified DRR with negative deficit for packet scheduling in routers”,

ARSSS Int. Conf. ICNCCT, Paper id: IM-NCCT-LNVL-11028-108, **Feb. 2018**

[12] Z.M.Patel, “Performance evaluation of configurable Viterbi decoder for wireless network”, ARSSS Int. Conf. ICNCCT, Paper id: IM-NCCT-LNVL-11028-109, **Feb. 2018**

[13] Naveen K. Kabra, Z.M.Patel, “Low power and High Speed Configurable ALU”, Int. Conf. on Innovations in Electronics and Communication Engineering ICIECE (Springer), Proceedings of the 7th ICIECE 2018. Vol. 65, pp. 355-363, **Aug. 2018**.

[14] Naveen K. Kabra, Z.M.Patel, “Low Power Radix-8 Modulo 2n + 1 Multiplier Using Modified Weighted Method”, Springer Proceedings in Advances in VLSI and Embedded System (AVES 2019), Vol. 676, pp.183-200, **Dec. 2019**

[15] Z.M.Patel and Harshal Prajapati, “High Speed Divide by ¾ Pre-scalar”, 5th IEEE conference ICEECCOT 2021, pp.662-664, **Dec. 2021**

[16] Deergha Agarwal and Z.M.Patel, “Comparitive Analysis of Matching Networks for Low Noise Amplifier design using ASM GaN HEMT for Ka Band”, IEEE GlobConPT 2022, pp.1-5, **Sept. 2022**

[17] Prajakta More and Zuber Patel, “LoRaWAN Performance Analysis with Data Rate”, IEEE conf. ICCEE-23 at MIT-ADT Pune. **27-29 April, 2023** (Scopus), https://doin.org/10.1109/ ICCCEE55951.2023.10424626

[18] Deergha Agarwal and Z.M.Patel, “2.5WClass-F Power Amplifier using Balanced Stub Harmonics on 150 nm GaN HEMT device for 5G Applications”, IEEE Conf. on DevIC, pp.661-669, **April, 2025**
doi: 10.1109/DevIC63749.2025.11012296

ANNEXURE –B :

Expert Talks Delivered

[1]. An expert lecture on "Low power VLSI design" in MINDBEND Feb., 2007 at SVNIT.

[2]. Expert talk on "FPGA design implementation flow" during National Workshop on 1Mar., 2009 at SVNIT.

[3]. "Introduction to VHDL", (IETE Student Forum Workshop) ISF workshop, SVNIT, Sept. 2010

[4]. "Behavioral modeling using VHDL", (IETE Student Forum Workshop) ISF workshop, SVNIT, Sept. 2010

[5]. "Embedded System – A Design Guide" at Parul Institute of Technology., Vadodara (Gujarat State), 15th Mar. 2014

[6]. Two Expert Talks (1.5Hrs) on "Arithmetic Building Block-I" and "Arithmetic Building Block-II" in QIP short term course on Digital VLSI Design on 22-23 Dec. 2016 at SVNIT.

[7]. Two talks (i) Analog VLSI Design (ii) MOS opamp circuits in short term training program (STTP) on 26-30 Dec. 2018 at SVNIT

[8]. Talks on (i) VLSI Design of Multipliers (ii) Logic Architectures for Dividers circuits in short term training program (STTP) on 26-30 Dec. 2018 at SVNIT

[9]. Two lectures in FDP on Digital CMOS Circuits and Devices, Electronics and ICT Academy, MNIT Jaipur.22-26 May, 2018

[10]. Expert lecture (2.5 Hrs) on "MCU and RTOS for Embedded Systems" at G H Raisoni Institute of Engineering & Technology, Nagpur 4th Oct., 2021

[12]. Expert Lecture on "Embedded Systems: Technology and Trends", MIT - ADT University, Pune, 25 Mar., 2023