RESUME

NAME : Zuber M. Patel

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1. Personal profile:

Name	:	ZUBER M. PATEL
Date of birth	:	02-09-1975
Father's name	:	M. A. PATEL
Sex	:	Male
Marital status	:	Married
Languages known	:	English, Hindi, Gujarati
Nationality	:	Indian
Permanent address	:	201, Evergreen Complex – B Wing, Morabhagal, Rander Road, Surat – 395005. Gujarat. INDIA mobile: +919898698793

2. Education:

Course	Discipline	Institution	Grade
12TH Std.	Science	Gujarat Board, Gujarat	Distinction
Bachelor of Engg. (Electronics)	Electronics	NIT (formerly REC), Surat, Gujarat. India	Distinction
M. Tech (Electrical)	Microelectronics & VLSI	I I T, Bombay, India	9.29 /10 CGPA
PhD	Scheduling in Wireless Broadband Networks	NIT Surat. Gujarat. India	N.A.

3. TOTAL EXPERIENCE: (Total 21 years 5 months) as on Mar.,2021

(Teaching: 19 Years 5 Months, Industry: 2 Years)

- **Present Employment:** (**18** years **6** months)

Associate Professor, Electronics Engg**.** Dept., **S.V. National Institute of Technology (SVNIT)**, Surat, India. (www.svnit.ac.in)

- Teaching in Electronics & Communication engineering courses
- Guiding and Handling the UG and PG projects/dissertations
- Managing laboratories as a Laboratory In charge
- Perform instructionally related duties such as curriculum development, program outcomes assessment, student advising and mentoring.
- Engage in research projects and development

- **Previous Employment 1:** (**11** months)

Faculty, Electronics Engg. Dept., Nirma Institute of Diploma Studies, Ahmedabad, India, Sept. 2001 to Aug. 2002

- Teaching in Electronics engineering subjects
- Allied works related to academics and administration

- **Previous Employment 2:** (**2** years **3** Months)

System and Network Administrator, CMS Computers, Surat.
Dec.1998 – Mar. 2001

- Computer hardware, networking and administration using Network OS.
- Windows Servers and Workstations management
- LAN/WAN installation with switches, hubs and bridges.

4. PUBLICATION/ RESEARCH WORK:

- **10** International Journal and **14** International Conference Publications.
- **Co-coordinator** of **Research Project** named VLSI SMDP-II from MCIT, Govt. of India. The research project was related to VLSI Design and for the duration of **5 years (2006-2011** extended up to Mar. 2013**).**
- Member of Investigators of **C2SD Research Project (**Duration: **5 years** i.e. **2016 to 2021)** from MeitY, Govt. of India. In this project, I am involved in ASIC design for Error-Correcting Codec for low power high speed serial transceiver for space application.
- **PhD** work was based on Design, Development and Implementation of Novel Packet Scheduling Algorithms for wireless broadband network for uplink and downlink transmissions.
- **M.Tech Dissertation** was based VLSI (FPGA & ASIC) implementation of 802.16 baseband processing (scrambling, interleaving, error correcting codec, mapping etc.)

5. Research Interests:

- Digital System Design
- RISC Processors and SoC
- Embedded System Design
- Low Power design of Wireless transceiver PHY Layer

5. Courses Presently Handled:

- Embedded Systems, ARM microcontrollers
- Digital Logic Design
- Analog VLSI Design

5. SKILLS:

- Assembly and embedded C programming for embedded system
- HDL/FPFA based design with ModelSim and Xilinx ISE
- Cadence/Synopsis tool set related to ASIC design
- Linux/Windows OS, C/C++ programming

Declaration:

I hereby declare that the information furnished above is true to the best of my knowledge. I am liable to be rejected if at any point it is found to be incorrect.

Dr. Z. M. PATEL

Dept. of Electronics Engg.,

SVNIT (http://www.svnit.ac.in/web/department/electronics/faculty_eced.php),

Surat. India

APPENDIX – A Publications

Total Publications= 14 (Int. conf.) +10 (Int. Journals) = **24**

[1] PhD Publications:

International Journals:

[1]. Z.M.Patel and U.D.Dalal, ―Design and Implementation of Low Latency Weighted Round Robin (LL-WRR) Scheduling for High Speed Networks,‖ International Journal of Wireless and Mobile Networks (IJWMN) AIRCC Pub., vol. 4, no. 6, **Aug. 2014**

[2]. Z.M.Patel and U.D.Dalal, "Enhancing Performance of Internetworking with Novel RED-AT Congestion Control Algorithm," International Journal of Scientific and Engineering Research (IJSER) Pub., vol.5, no. 11, **Nov. 2014.**

[3]. Z.M.Patel and U.D.Dalal, "Implementation and Evaluation of Dynamically Weighted Low Complexity Fair Queuing (DWLC-FQ) Algorithm for Packet Scheduling in WiMAX Networks," International Journal of China Communications (SCI Journal-Cosponsored by IEEE ComSoc and CIC**),** Accepted: 14 Sept. 2015, Published: **May 2016**

International Conferences:

[1]. Z.M.Patel and U.D.Dalal, "Implementation and Analysis of Downlink scheduling for 802.16 networks using Controlled Priority Queuing (CPQ)," in proceeding of SPRINGER International Conf. on Advanced Computing (ICAdC 2012), vol.174, pp.399-406, **July 2012.**

[2]. Z.M.Patel and U.D.Dalal, "Performance Evaluation and Comparison of Queue Scheduling Schemes for WiMAX under Heterogeneous Traffic," in proceedings of IEEE International Conf. Circuits, Controls and Communication (C3 2013)**,** paper ID:100, **Dec. 2013.**

[3]. Z.M.Patel and U.D.Dalal, "Improved CAC Scheme for WiMAX with Adaptive Bandwidth Reservation and Degradation Policy," in proceedings of International Conferenc**e** on Computer, Electrical & Electronics Engineering (CEEE'15), Phuket, Thailand. paper ID:100, 3-4 **Oct. 2015**

[2] Publications Outside PhD Study:

International Journals:

[1] Kinnar G. Vaghela and Z.M.Patel; "Optimizing performance of Spectrum Subtraction using the Time Frequency Filtering"; International Journal of Research and Reviews in Electrical and Computer Engineering (IJRRECE) ; Vol. 1, No. 2; Science Academy Publisher, UK. ISSN: 2046-5149; **Mar. 2011**

[2] Nilesh Ranpura, Prof. Z.M.Patel and Ekta Mehul; "Simulation of unified architecture of IEEE 802.11a and 802.16a PHY layers using MATLAB" ; International Journal of Computer Science & Emerging Technologies ; Vo.2, No.2 ; ISSN: 2044-6004 ; **April 2011**

[3] Kinnar vaghela and Prof. Z.M.Patel ; "Optimized Technique for Speech Noise Elimination using Traditional Spectrum Subtraction" ; IUP Journal of Telecommunication ; Vol.3, No.2 ; ISSN: 0975-5551 ; **May 2011**

[4] Jignesh Oza, Z.M.Patel, Upena Dalal & et. al. ; "Optimized configurable OFDM design blocks for Wi-Fi and Wi-Max" ; International Journal of Research and Reviews in Electrical and Computer Engineering (IJRRECE) ; Vol.1, No.3 ; Science Academy Publisher, UK. ISSN: 2046-5149 ; **Sept. 2011**

[5] Z.M.Patel, "Low Noise and Low Distortion Telescopic OTA for Biomedical Signal Processing", Journal of Recent Advances in Electrical & Electronic Engineering, Bentham Science Publishing ; Vol.12, No.1 ; Bentham Science Publishing, UK. ISSN: 2352-0973; Accepted: 2nd July, 2018, Published: **Dec. 2018**

[6] Navin Kabra and Z. M. Patel, "Novel Approach to Design Hard Multiple Generator for Radix-8 Modulo 2n-1 Multiplier using Inclusive-OR Adder", Integration, the VLSI Journal, Elsevier (SCI), ISSN: 0167-9260, Published: **25 July, 2020**

[7] Navin Kabra and Z. M. Patel, "Radix-8 Modulo 2n Multiplier Using Area and Power Optimized Hard Multiple Generator", Computers and Digital Techniques. IET (SCI), ISSN: 1751-861X, Published: **13 Dec., 2020**

International Conference:

[1] Jignesh Oza, Z.M. Patel, Nilesh Ranpura & et. al. ; "Optimized Configurable Architecture of Modulation Techniques for SDR applications." ; International Conference on Coumputer & Communication Engg. (ICCCE'10) ; ISBN: 978-1-4244-6235-3 ; pp. 494-498 ; IEEE ; **May 2010.**

[2] Devashish Raval, Z.M. PateL,Nilesh Ranpura and Ekata Mehul ; "Comparative Analysis of OFDM parameters in WiFi and WiMAX Technologies" ; International Conference on Signals, Systems and Automation (ICSSA 2011) ; GCET, **Jan. 2011**

[3] Z.M.Patel, "Power and Area Efficient Hardware Architecture for WiMAX Interleaving"; International Conference on Communication and Signal Processing, ICCSP 2014, Bangkok ; paper ID: SP0020 ; IACSIT ; **Oct. 2014**

[4] Z.M.Patel, "Enhancing Speed and Reducing Power of Shift and Add Multiplier', International Conference on Communication and Signal Processing (ICCSP), Thailand, Publisher: Research World, ISBN: 978-93-85973-31-4, 12-13th **April, 2016**

[5] J.R.Prajapati and Zuber M. Patel, "High linearity low noise figure mixer for Wi-max in 0.18 μm tsmc technology", In Proc. of IEEE Conference on "Signal and Information Processing (IConSIP)", DOI: 10.1109/ICONSIP.2016.7857456, **Oct. 2016**

[6] Z.M.Patel, "Queue occupancy estimation technique for Adaptive threshold based RED", **IEEE** conf. on ICCS, , pp. 437-440, DOI: 10.1109/ICCS1.2017.8326038, **Dec. 2017**

[7] Z.M.Patel, "Configuratble Mapper and Demapper for Physical Layer of SDR based wireless transceiver", Springer ICCCPE **2018**, DOI:10.1007/978-981-13-0212-1, **Jan. 2018**

[8] Z.M.Patel, "Modified DRR with negative deficit for packet scheduling in routers", ARSSS Int. Conf. ICNCCT, Paper id: IM-NCCT-LNVL-11028-108, **Feb. 2018**

[9] Z.M.Patel, "Performance evaluation of configurable Viterbi decoder for wireless network", ARSSS Int. Conf. ICNCCT, Paper id: IM-NCCT-LNVL-11028-109, **Feb. 2018**

[10] Naveen K. Kabra, Z.M.Patel, "Low power and High Speed Configurable ALU", Int. Conf. on Innovations in Electronics and Communication Engineering ICIECE **(Springer)**, Proceedings of the 7th ICIECE 2018. Vol. 65, pp. 355-363, **Aug. 2018.**

[11] Naveen K. Kabra, Z.M.Patel, "Low Power Radix-8 Modulo $2^n + 1$ Multiplier Using Modified Weighted Method", Springer Proceedings in Advances in VLSI and Embedded System (AVES 2019), Vol. 676, pp.183-200, **Dec. 2019**

ANNEXURE –B : STTP and Workshop Participated

STTPs:

1. One week on "Helping Students Develop Better Learning Skill & Habit for Human Value in Education" at SVNIT from 21ST to 26TH June-2004
2. Two weeks on "Digital Design using FPGAs/CPLDs" from 6 to 16 Dec., 2004 at Nirma Inst. of Tech., Ahmedabad.
3. Two weeks on "Low Power VLSI design" from 11 to 22 Sep.,2006 at IIT, Kharagpur
4. One week on "FPGA Laboratory" at IIT Delhi from 13 to 17 july 2009.
5. Two weeks Summer school on "Basic Electronics", IIT Bombay, June 2011.

National Workshops:

1. Two Day Workshop on " Challenges in VLSI", 21 & 22nd Dec.,2006 at DAIICT
2. Three day National workshop on "Recent Trends in microelectronics and VLSI" 24 to 26 May,2007 at SGSITS, Indore
3. Two day National Workshop on "Low Power VLSI Design", at Nirma University, 29-30 Jan, 2010.
4. Two day IUCEE workshop on "FPGA embedded system", 8-9 July. 2011 at BVRIT Hyderabad.
5. National workshop on NS-2, MIT, Anna University,Chennai. 2-3 Dec., 2011

ANNEXURE –C :

Expert Talks:

[1]. An expert lecture on "Low power VLSI design" in MINDBEND Feb., 2007 at SVNIT.

[2]. Expert talk on "FPGA design implementation flow" during National Workshop on 1Mar., 2009 at SVNIT.

[3]. "Introduction to VHDL", (IETE Student Forum Workshop) ISF workshop, SVNIT, Sept. 2010

[4]. "Behavioral modeling using VHDL", (IETE Student Forum Workshop) ISF workshop, SVNIT, Sept. 2010

[5]. "Embedded System – A Design Guide" at Parul Institute of Technology., Vadodara (Gujarat State), 15th Mar. 2014

[6]. Two Expert Talks (1.5Hrs) on "Arithmetic Building Block-I" and "Arithmetic Building Block-II" in QIP short term course on Digital VLSI Design on 22-23 Dec. 2016 at SVNIT.

[7]. Two talks (i) Analog VLSI Design (ii) MOS opamp circuits in short term training program (STTP) on 26-30 Dec. 2018 at SVNIT

[8]. Talks on (i) VLSI Design of Multipliers (ii) Logic Architectures for Dividers circuits in short term training program (STTP) on 26-30 Dec. 2018 at SVNIT

[9]. Two lectures in FDP on Digital CMOS Circuits and Devices, Electronics and ICT Academy, MNIT Jaipur.22-26 May, 2018