Name: Anand D. Darji

Date of Joining: 1st August, 2000

Qualification: Ph.D. (Microelectronic),
Department of Electrical Engineering, IIT Bombay
M.Tech (Electronic Systems), IIT Bombay (CPI 9.02)
B.Tech (Electronics), Birla Vishvakarma Mahavidyalaya (B.V.M) Engineering College, Sardar Patel University, Vallabh Vidyanagar, Gujarat

Designation: Assistant Professor, Electronics Engineering Department

Research Interest: VLSI Design, FPGA-based systems design, VLSI DSP architecture, Embedded System Design, Electronics Instrumentation, Signal Processing, Bio-medical Signal/image processing

Research Publications:

a) International Journals

1. A.D.Darji, Arun R., S. N. Merchant, A. N. Chandorkar, ``Multiplierless Pipeline Architecture for Lifting-based 2-D Discrete Wavelet Transform," J. IET Computers & Digital Tech., Manuscript ID: CDT-2013-0167 (Accepted)

2. High-performance hardware architectures for multi-level lifting-based discrete wavelet transform Anand D Darji, Shailendra Kushwah, Shabbir N Merchant, Arun N Chandorkar *EURASIP Journal on Image and Video Processing* 2014

3. A. D. Darji, S. Agrawal, A. Oza, V. Sinha, A. Verma, S. N. Merchant, A. N. Chandorkar, "Dual-scan Parallel Flipping Architecture for Lifting-Based 2-D Discrete Wavelet Transform," IEEE Trans. Circuits Syst. II : Express Briefs, vol. 61, no. 6, pp. 433-437, Jun. 2014

4. A.D. Darji, T.C. Lad, S.N. Merchant, A.N. Chandorkar," Watermarking Hardware Based on Wavelet Coefficients Quantization Method", Springer Journal of Circuits, Systems, and Signal Processing, vol. 32, , no. 6, pp. 2559-2579, Dec. 2013

5. Kaushal Buch, Anand Darji, "Interpolated histogram method for area optimized median computation", International Journal of Electronics, Taylor and Francis, Vol.5, pp. 468-472, Apr. 2013

6. Taral D. Chhatbar, Anand Darji ,"FPGA Implementation of 2048-Point FFT/IFFT High speed Architecture", International Journal of emerging Technologies in Engineering Technology and Sciences,Vol.2,No.2 ,pp.785-788, 2009

7. Amit Joshi, Anand Darji," Secure Digital Camera With DWT based Watermarking," "International Journal of emerging Technologies in Engineering Technology and Sciences,Vol.2,No.2 ,pp.813-818, 2009

b) International Conferences

1. A. D. Darji, A. Limaye , "Memory efficient VLSI architecture for lifting-based DWT," IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), 3-6 Aug. 2014, College Station, Texas, pp. 189-192

2. A.D. Darji, K. Shashikanth, A. Limaye, S. N. Merchant, A. N. Chandorkar, "Flipping-based high speed VLSI architecture for 2-D lifting DWT," IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), 3-6 Aug. 2014, College Station, Texas, pp.193-196

3. Darji, A.; Shukla, S.; Merchant, S.N.; Chandorkar, A.N., "Hardware Efficient VLSI Architecture for 3-D Discrete Wavelet Transform," 27th International Conference on VLSI Design, IIT Bombay, pp.348-352, 5-9 Jan. 2014

4. A. D. Darji, T. Doodi, N. S. Manogana, N. Meena, A. Ojha, A. N. Chandorkar, S. N. Merchant, "Boundary treatment analysis of 2-D DWT using lifting (9,7) filter with fixed point arithmetic for hardware implementation," In Proc. 2012 Annual IEEE India Conference (INDICON), Rajagiri School of Engineering & Technology, Kochi, 7-9 Dec. 2012, pp. 903-908

5. A. D. Darji, Nisarg Trivedi, S. N. Merchant, A. N. Chandorkar, "Hardware efficient recursive VLSI architecture for multilevel lifting 2-D DWT," In Proc. 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, 20-23 May 2012, pp. 1014-1017

6. T. C. Lad, A. D. Darji, S. N. Merchant, A. N. Chandorkar, "VLSI Implementation of Wavelet Based Robust Image Watermarking Chip," In Proc. 2011 International Symposium on Electronic System Design (ISED), Rajagiri School of Engineering & Technology, Kochi, 19-21 Dec. 2011, pp. 56-61

7. A. Darji, S. N. Merchant, A. N Chandorkar, "Efficient pipelined VLSI architecture with dual scanning method or 2-D lifting-based Discrete Wavelet Transform," In Proc. 2011 13th International Symposium on Integrated Circuits (ISIC), Nanyang Technological University, Singapore, 12-14 Dec. 2011, pp. 329-331

8. A. D. Darji, R. Bansal, S. N. Merchant, A. N. Chandorkar, "High speed VSLI architecture for 2-D lifting Discrete Wavelet Transform," In Proc. 2011 Conference on Design and Architectures for Signal and Image Processing (DASIP), Tampere, Finland, 2-4 Nov. 2011, pp. 1-6

9. A. M. Joshi, A. Darji, V. Mishra, "Design and implementation of real-time image watermarking," In Proc. 2011 IEEE International Conference on Signal Processing, Communications and Computing (ICSPCC), Northwestern Polytechnical University, Xi'an, Shaanxi, China, 14-16 Sept 2011, pp. 1-5

10. P. Pokharel, B. Bhatta, A. D. Darji, "Optimized drivers for PS/2 and VGA using HDL," In Proc. 2011 IEEE International Conference on Computer Science and Automation Engineering (CSAE), Shanghai, China, 10-12 June 2011, pp. 262-266

11. A. D. Darji, M. S. Patil, "VLSI Implementation of Balanced Binary Tree Decomposition Based 2048-Point FFT/IFFT Processor for Mobile WI-Max," In Proc. IEEE 3rd International Conference on Emerging Trends in Engineering and Technology (ICETET), BITS Pilani, Goa, 19-21 Nov. 2010, pp. 745-748

12. A. Darji, A. N. Chandorkar, S. N. Merchant, V. Mistry, "VLSI Architecture of DWT Based Watermark Encoder for Secure Still Digital Camera Design," In Proc. IEEE 3rd International Conference on Emerging Trends in Engineering and Technology (ICETET), BITS Pilani, Goa, 19-21 Nov. 2010, pp. 760-764

13. M. S. Patil, T. D. Chhatbar, A. D. Darji, "An area efficient and low power implementation of 2048 point FFT/IFFT processor for mobile WiMAX," In Proc. IEEE International Conference on Signal Processing and Communications (SPCOM), IISC Bangalore, 18-21 July 2010, pp. 1-4

14. T. D. Chhatbar, A. D. Darji, "High Speed High Throughput FFT/IFFT Processor ASIC for Mobile Wi-Max," In Proc. IEEE 2nd International Conference on Emerging Trends in Engineering and Technology (ICETET-09), C. H. Raisoni College of Engineering, Nagpur, 16-18 Dec. 2009, pp. 402-405

15. A. M. Joshi, A. D. Darji, "Efficient Dual Domain Watermarking Scheme for Secure Images," In Proc. International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom '09), Kottayam, Kerala, 27-28 Oct. 2009, pp. 909-914

16. Ketki Joshi, A. D. Darji, U. D. Dalal, "Design and Analysis of Low power VITERBI Decoder For CDMA Communication System," In Proc. 13th IEEE / VSI VLSI Design And Test Symposium (VDAT-2009), Wipro Campus, Electronic City, Bangalore, 8-10 July 2009, pp. 358-369

17. Hiren Mewada and Anand Darji, "Reconfigurable Implementation of New Millennium Standard JPEG 2000," In Proc. IEEE International Conference on Advanced Electrical, Electronics, Communication and Information Technology (Indicon 2007), Central Power Research Institute (CPRI), Bangalore, 6-8 Sept. 2007

c) National Conferences

1. Vipul Mistry, Anand Darji, " Hardware implementation of DWT/IDWT Processor", Indian conference on Computer vision, Graphics, Image and Video Processing, R.K. Nehru Engineering College, Nagpur, March 13-14, 2009

2. Amit M Joshi, Anand Darji, Taral D Chhatbar, Abhishek Aghrahari," Clock skew analysis and optimization of sequential circuit", NCIS 07,M.J.College of Engineering and Technology, Hyderabad, 24-25 August, 2007

3. Taral chhatbar and Anand Darji, "A Comparative Study of FFT Algorithms and Implementation on FPGA" Emerging Trends in Communication & Computing (ETCC) at NIT, Hamirpur, 27-28 July, 2007

4. Anand Darji and Hiren mewada , "Recent Trend in Data Compression using Wavelet" , National Conference on Engineering Trend in Electronics (NCETE) at MAE Pune, 28-29 Dec,2006, pp.221-226

Research Grant/Project

1. Modernization of Digital Signal Processing Lab, Funding Agency MHRD, Project Duration : 2 Year, 4.5 Lacs
2. Special Manpower Development Project for VLSI Design and Related Software , Project Duration 5 Years, 1 Crore

Consultancy Report:

Anand Darji and S.C. Patwardhan; "Performance Analysis of Zigbee (IEEE 802.15.4) enabled wireless sensor network for Control Applications"; Consultancy Report for Honeywell Technological Solution Limited, Bangalore; 2006 (Research Work done at Automation Lab, IIT Bombay)

Expert Lectures:

a) Expert Lecture at outside SVNIT

1. Expert Lecture on "Wireless sensor Network " at STTP – Recent trend in embedded systems", SCET, Surat (Dt: 20/12/2006)
2. Expert Lecture on "Interfacing I/O" at Udbhav-2007 CKPCET, Surat (Dt: 23/2/2007)
3. Expert Lecture on " ZIGBEE: Wireless sensor network for Automation" at STTP Advanced control system at DDIT, Nadiad.
4. Expert Lecture on " Embedded Software Architecture" , ISTE-STTP on VLSI and Embedded Systems: Design and Applications, SCET ,Suart , 9-14 May, 2008
5. Expert Lecture on " Embedded System Development Cycle : A Case study on 3-Phase Heater Controller, ISTE-STTP on VLSI and Embedded Systems: Design and Applications, SCET ,Suart , 9-14 May, 2008
6. Expert Lecture on " Introduction to VLSI Design ", E-infochips , 1st oct, 2010, Ahemdabad,2011
7. Expert Lecture on " Design Techniques for Low Power VLSI Design ",1st oct, 2010, E-infochips , Ahemdabad, 2011
8. Lecture Series on Semiconductor Physic and MOS Structure, MOSFET operation and Characteristics, MOSFET Scaling and Short Channel Effects, CMOS fabrication Steps and Layout, CMOS inverter and Logic Gate Design, 28th Feb, 2012, E-eInfochips Academic Initiative, Eitra, Ahemdabad
9. PLD Architectures, Maliba Institue of Techology, Surat, 20th April, 2013
10. FPGA based system Design Flow, Tapi Institute of Technology, Surat , 27th April, 2013
11. DSP Algorithms to Implementations, STTP on Digital Signal Processing and Applications, Parul Institute of Engineering and Technology, 16-20 Dec. 2013
12. Memory Architecture in Nanometer Regime, AICTE Sponsored Two days National Seminar in VLSI, Parul Institute of Engineering and Technology, 17th-18th Jan. 2014
13. Research Scope in VLSI Design, A workshop on Research Trend in VLSI, Parul Institute of Engineering and Technology, 15th March, 2014
14. Hardware Efficient Implementation of Video Capsule Endoscopy, NIT Kurukshetra, 15 Nov, 2014

b) Expert Lecture at SVNIT

1. Expert Lecture on " Hard ware Description language " at Mindbend 2007, SVNIT
2. SPICE and Magic CAD tool , Faculty Development Program sponsored by TEQIP , 15-19 Dec 2008
3. LIFE with SPICE, National Workshop on VLSI Design tools sponsored by SMDP-II Project ,Department of Information Technology (DIT), New Delhi, Feb 28- March 1 , 2009
4. Integrated circuit (IC) Design flow, National Workshop on VLSI Design tools sponsored by SMDP-II Project ,Department of Information Technology (DIT), New Delhi, Feb 28- March 1 , 2009
5. Expert Lecture on ADC-Architectures , AICTE Sponsored STTP on Microcontrollers and Applications, 14-18 Dec, 2009
6. Algorithm to implementation, AICTE Sponsored STTP on Microcontrollers and Applications, 21-25 Dec, 2009
7. Introduction to HDL, IETE Organized and SMDP-II Sponsored Workshop on HDL,18-19 Sept., 2010
8. Introduction to Xilinx ISE, IETE Organized and SMDP-II Sponsored Workshop on HDL, 18-19 Sept.,2010
9. Nanoscale memory architectures, TEQIP-II Sponsored STTP on Nanoscale Integration, Fabrication and Characterization, 21-25 Oct., 2013

STTPs/Conferences Organized:

National Workshop on VLSI Design tools, 28 Feb-1 March, 2009, SVNIT Surat.

Administrative Responsibilities:

a) Current:
PG In-Charge M. Tech (VLSI & Embedded System) specialization, Lab In-charge VLSI Design Lab, Department Academic Advisory Committee (DAAC) secretary.

b) Past:
Co convener of Mindbend-2008, Faculty Advisor of IETE Student chapter, In-charge Electronics System Design lab.

Other Information:

I have done Ph.D. in the field of Microelectronics from Department of Electrical Engineering, IIT Bombay under the guidance of Prof. A.N. Chandorkar and Prof. S.N.Merchant. I am life member of ISTE and IEEE Society. I have guided 15 M.Tech Dissertations, 40 B.Tech Projects, 55 B.Tech Seminars.
A chip for 2048 Point FFT/IFFT processor using UMC 180 nm technology is designed under SMDP-II project India-chip program.