डिपार्टमेंट ऑफ़ इलेक्ट्रॉनिक्स इंजीनियरिंग
DEPARTMENT OF ELECTRONICS ENGINEERING
सरदार वल्लभभाई नेशनल इंस्टिट्यूट ऑफ़ टेक्नोलॉजी, सूरत
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT

क्रमांक:DECE/ISRO / / 2025-26 दिनांक:12/08/2026

Recruitment of Project Staff on Purely Contract Basis

Applications are invited in the prescribed format for the post of Research Associate-I (RA-I) or Project Associate–I on purely contract basis in the Department of Electronics Engineering, Sardar Vallabhbhai National Institute of Technology, Surat, Gujarat, India as per the details mentioned below:

Title of the project	Algorithm Development For Detection of Spoofing Signals in NavIC Receivers (**FPGA**-Based)
Funding Agency	RESPOND, ISRO
Name of the post	**Research Associate-I (RA-I) or Project Associate-I (PA-I)** The upper age limit for "Research Associate-I" and "Project Associate-I" is 35 years. The fellowship amount and all other service conditions of the Research Associate-I and Project Associate-I are as per the DOS order No. A 12011/12/2020-Sec I dated October 13, 2020
Number of posts	01 (One)
Duration	Research Associate-I or Project Associate-I: 03 Years or till the completion of the project, whichever is earlier. Initial appointment will be for one year, extendable by 2 more years on annual basis. The extension would be based on the satisfactory performance of the RA-I or PA-I and possible extension of the project.
Consolidated Pay	RA-I: Rs. 58,000/- p.m. + 20% HRA PA-I: Rs. 31,000/- p.m. + 20% HRA
Last date/time of submission of application	**18 August 2026**
Essential Qualification	**Research Associate-I (RA-I):** 1. Ph.D. in Electronics Engineering or equivalent degree OR 2. having 3 years of research, teaching and design and development experience after M. E. / M. Tech in **VLSI** Design / Microelectronics / Microelectronics and **VLSI** Design / Electronics & Communication / or equivalent degree with at least one research paper in Science Citation Indexed (SCI) journal **Project Associate–I(PA-I):** 1. M. E. / M. Tech in **VLSI** Design / Microelectronics / Microelectronics and **VLSI** Design / Electronics & Communication / or equivalent
Desired skills	1. **FPGA** design and development, **VHDL/Verilog** Programming Software Skills: **Xilinx Vivado**, MATLAB, C/C++, Python etc. 2. Basic GNSS receiver, signal processing, embedded computing, communication systems, etc.

How to apply:
The application form and the details of all educational qualifications and relevant experience required for this position is available on Institute website http://www.svnit.ac.in**.** Duly filled and signed application form along with self-attested scanned copies of B. E. /B. Tech/ M. E. /M. Tech. / M. Sc. / Ph. D. mark-sheets of all semesters, relevant experience certificates and other necessary documents if any must be submitted as a single PDF file by email at snshah@eced.svnit.ac.in on or before **18 August, 2026**. Applications received after said date will not be considered. *Kindly also bring relevant documents of the same (Original and Xerox) at the time of the interview.*

फ़ोन नं: संस्थान कार्यालय: २२२३३७१-७४, फैक्स नं:२२२८३९४,२२२७३३४ विभागीय प्रमुख: २२०१५५१, विभाग कार्यालय: २२०१५५२
ई-मैल: director@svnit.ac.in, hod@eced.svnit.ac.in

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Please Note:

1. The above position is purely contractual for one year and can be extended till project duration based on the performance evaluation every year. The above-mentioned qualifications are minimum requirements. In case of large number of applications additional short-listing criteria may be applied by the selection committee.
2. Candidates having minimum aggregate First Class/CGPA 6.5 for all qualified degrees and B. E. /B. Tech/ M. E. /M. Tech. / M. Sc. / Ph. D. can only apply. The candidates with relevant experience will be given preference.
3. The list of short-listed candidates will be displayed on the institute website.
4. The selected candidate will be intimated via email.
5. An applicant must ensure the authenticity of information provided in support of experience claimed, other documents and photograph.
6. No TA/DA will be paid for appearing in the interview and/or joining the position.
7. Candidate employed in institute/Industry must produce No-Objection Certificate (NOC) at the time of interview.
8. Candidates who got selected may be allowed to enroll for Ph.D. program subject to the fulfillment of eligibility conditions of SVNIT, Surat.
9. The candidate completing the research work will be provided by the experience certificate by the Project Investigator and Recommendation letter, if required.
10. **Date of Interview: 19 August 2026**

Director,
SVNIT, Surat

फ़ोन नं: संस्थान कार्यालय: २२२३३७१-७४, फैक्स नं:२२२८३९४,२२२७३३४ विभागीय प्रमुख: २२०१५५१, विभाग कार्यालय: २२०१५५२
ई-मैल: director@svnit.ac.in, hod@eced.svnit.ac.in