डिपार्टमेंट ऑफ़ इलेक्ट्रॉनिक्स इंजीनियरिंग
DEPARTMENT OF ELECTRONICS ENGINEERING
सरदार वल्लभभाई नेशनल इंस्टिट्यूट ऑफ़ टेक्नोलॉजी, सूरत
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT

क्रमांक:**DECE/DST/ / 2024-25** दिनांक:**23/04/2024**

Recruitment of Project Staff on Purely Contract Basis

Applications are invited on prescribed format for the post of Junior Research Fellow on purely contract basis for one year (may be extended further) for DST, Government of India, New Delhi sponsored project entitled "Design and Development of MEMS-based portable platform with ionselective Self-Assembled Monolayer SAMs for the detection of toxic Heavy Metal Ions HMIs in ground water" at the institute. The application form and the details of all educational qualifications and relevant experience required for various positions are available on Institute website http://www.svnit.ac.in**.** Duly filled and signed application form along with self-attested scanned B.Tech./ M.Tech. / Ph. D. mark-sheets of all semesters/ Score card of CSIR-UGC NET/GATE exams, relevant experience certificates and necessary documents must be submitted in a single PDF file by email at add@eced.svnit.ac.in to on or before **21st May, 2024**. Applications received after said date will be not considered.

Sr. No	Post	Qualification	Experience	No. of. Posts / Duration	Consolidated Pay (Per Month)
1.	JRF (Junior Research Fellow)	B. E. / B. Tech. (Electronics / Electronics & Communication) or equivalent **OR** M.E / M. Tech* in VLSI Design / Microelectronics / Microelectronics and VLSI Design or equivalent Qualified in National Level eligibility test CSIR-UGC NET/ GATE	**Familiarization with MEMS Fabrication Tools and processes:** Lithography, Sputtering, e-beam evaporation, wafer cleaning, Spin coating, Atomic force microscopy (AFM), Field Emission Scanning Electron Microscope FESEM/ Energy Dispersive X-ray (EDX), Fourier-transform infrared spectroscopy (FTIR), Raman spectroscopy. **Software:** Clevin, COMSOL Multiphysics (MEMS and Microfluidic module). **Embedded Systems Design**	1 Post/ 11 months	Rs. 37,000/- p.m. + 18% HRA

*Aggregate First Class /CGPA 6.5 in B. E. / B. Tech. and / OR M.E / M. Tech.

1. Candidate having minimum aggregate First Class/CGPA 6.5 in B.E / B.Tech and/OR M. E. /M.Tech. with qualified in National level eligibility test such as CSIR-UGC NET/GATE ecan only apply.
2. The above positions are purely contractual for 11 months and can be extended till project duration based on the performance evaluation every year.
3. The last date for receiving applications is **21st May, 2024.**
4. Institute will not be responsible for any postal delay.
5. Applications received after last date will not be considered.
6. The list of shortlisted candidates will be displayed on the institute website on **23rd May, 2024**.
7. Interview/Test for the shortlisted candidates will be held on **27th May, 2024.** However, ***final date/venue of Interview/Tests will be communicated through E-mail.***
8. An applicant has to ensure the authenticity of information provided in support of experience claimed, other documents and photograph.
9. The qualification and experience may be relaxed at any point of time by the Institute for otherwise exceptional candidates.
10. **No TA/DA will be paid for appearing in the Interview**.
11. Candidate employed in institute/Industry must produce No-Objection Certificate (NOC) at the time of interview.
12. List of selected candidates will be displayed on the institute website within one week after interview held.
13. Candidates who got selected may be allowed to enroll for Ph.D. program subject to the fulfillment of eligibility conditions of SVNIT, Surat.

DIRECTOR
SVNIT, Surat

DEPARTMENT OF ELECTRONICS ENGINEERING
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ICHCHHANATH, SURAT-395007 (GUJARAT)
website: www.svnit.ac.in

APPLICATION FORM

1.	Post applied for		Self Attested Photograph
2.	Name of the Candidate		
3.	Address of the Candidate		
4.	Father's Name		
5.	Date of Birth		
6.	Age as on last date of application	_____Years _____ Months _____ Days	
7.	Contact No. (Mobile)		
8.	Email Id.		

9. Educational Qualification (Photocopy of certificate/degree must be attached)

Qualification	**Subject/Discipline**	**Board/Institute /University**	**Year**	**% of marks/ CGPA obtained (Aggregate)**
10th or equivalent				
12th or equivalent				
Bachelor Degree				
Master Degree				
Ph.D.				
Master Degree Thesis Title				
Ph.D. Thesis Title				

8. Relevant Experience (Details of Employment in chronological order. Enclose a separate sheet duly authenticated under your signature if necessary)

Organization	**Post Held**	**From**	**To**	**Pay Drawn**	**Nature of Duties**

9.	**Total emoluments per month presently drawn.**	
10.	**Additional information if any, which you would like to mention in support of your suitability for the post, (attached separate sheet if necessary)**	

Declaration

I hereby declare that the information furnished above is true to the best of my knowledge and belief. If at any time it is found that I have concealed any information or have given any incorrect data, my candidature/appointment, may be cancelled/terminated, without any notice or compensation.

Place:
Date:

Signature of the Candidate