Pinalkumar J. Engineer

CONTACT INFORMATION

Associate Professor
Department of Electronics Engineering
Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat
P.O. Ichchhanath,
Surat, INDIA-395007
Work: +91-261-220-1696
E-mail: pje@eced.svnit.ac.in
URL: https://www.svnit.ac.in/Data/facup/pjengineer/index.html

RESEARCH INTERESTS

Accelerated computing Edge Computing, Application Specific Processor Design, Energy-efficient Computing, VLSI architecture for real-time signal/image processing/AI/ML, High performance embedded computing.

ACADEMIC APPOINTMENTS

Associate Professor
Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat — Dec-2023 to present

Assistant Professor
Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat — Jan-2007 to Dec-2023

Assistant Professor
Charusat University of Science & Technology — Aug-2003 to Jan-2007
(Formerly, Charotar Institute of Technology, Changa)

Lecturer (Temporary)
M S University of Baroda — Aug-2001 to Aug-2003
Faculty of Technology & Engineering

EDUCATION

Ph.D. — 2019
Indian Institute of Technology Bombay
Title: *FPGA based scalable architectures for compute-intensive and communication-intensive multimedia applications*
Supervisors: *Prof. Rajbabu Velmurugan, Prof. Sachin Patkar*

M. E.(Microprocessor Systems & Applications) — 2002
M S University of Baroda

B.E.(Instrumentation & Control Engineering) — 1999
L D College of Engineering, Ahmedabad

RESEARCH PROJECTS

On-going:

[RP1] *PI:* **Pinalkumar Engineer**
Co-PIs: Anand Darji, Zuber Patel, Abhishek Acharya, Sandeep Mishra.
Title: Secure and Energy-efficient Mixed-domain Compute in memory-based AI accelerator Chip for Edge applications
Funding agency: Chips to Startup Programme, Ministry of Electronics and Information Technology, Government of India
Amount: 96 Lakhs
Duration: 5 Years from January-2024 .

Completed:

[RP1] *PI:* Anand Darji
Co-PIs: **Pinalkumar Engineer**, Jignesh Sarvaiya, Zuber Patel, Rasika Dhavse, Mehul Patel.
Title: Special Manpower Development Program for Chips to System Design (SMDP-C2SD).
Funding agency: Ministry of Electronics and Information Technology, Government of India
Amount: 87 Lakhs + Resources
Duration: February 2015- November 2021.

PATENTS

[PT3] **Pinalkumar Engineer**, Jignesh Patoliya and Hiren Mewada. *Novel ceramic 3D printing system*. Application No: 202321013954, Published, 17/03/2023.

[PT2] Hiren Mewada, **Pinalkumar Engineer**, and Sagar Patel. *A novel automated linear conveyor module robotic utility for pharmaceutical delivery using computer vision system*. Application No: 202311009969, Published, 17/02/2023.

[PT1] **Pinalkumar Engineer**, and Lokesh Sharma. *Dual Screen Mobile device with Solar Charging*. Application No: 201621010692, Granted on 03/09/2021, Term: 20 years from 29/03/2016.

REFEREED JOURNAL PUBLICATIONS

[J11] Hiren Mewada, Ivan Miguel Pires, **Pinalkumar Engineer**, Amit V. Patel. *Fabric surface defect classification and systematic analysis using a cuckoo search optimized deep residual network*. International Journal of Engineering Science and Technology (JESTECH), April-2024.
doi:https://doi.org/10.1016/j.jestch.2024.101681

[J10] Mitul Sudhirkumar Nagar, Sohan H. Patel, and **Pinalkumar Engineer**. *FPGA Based High-Speed Energy-Efficient 32-bit Fixed-Point MAC Architecture for DSP Application in IoT Edge Computing*. Journal of Circuits, Systems, and Computers (JCSC), March-2024.
doi:https://doi.org/10.1142/S0218126624502505

[J9] Mitul Sudhirkumar Nagar, Aditya Mathuriya, Sohan H. Patel, and **Pinalkumar Engineer**. *High-Speed Energy-Efficient Fixed-Point Signed Multipliers for FPGA-Based DSP Applications*. IEEE Embedded Systems Letters, January-2024.
doi:https://doi.org/10.1109/LES.2024.3364698

[J8] Akshay Parihar, Jigna B. Prajapati, Bhupendra G. Prajapati, Binti Trambadiya, Arti Thakkar, and **Pinalkumar Engineer**. *Role of IoT in healthcare: Applications, security & privacy concerns*. Intelligent Pharmacy, January-2024.
doi:https://doi.org/10.1016/j.ipha.2024.01.003

[J7] **Pinalkumar Engineer**, Rajbabu Velmurugan and Sachin B. Patkar. *Scalable implementation of particle filter-based visual object tracking on network-on-chip (NoC)*. Journal of Real-Time Image Processing, March-2019.
doi:https://doi.org/10.1007/s11554-018-0841-5

[J6] B Chandra Sekhar Naik, Anudeep J, Srinivas Lakavath and **Pinalkumar Engineer**. *FPGA Implementation of Earth Mover's Distance*. International Journal of Emerging Technology and Advanced Engineering, 4(6):June-2014.

[J5] Rahul V. Mehta, **Pinalkumar Engineer** and Milind S. Shah . *Multiple PicoBlazes-Review and Implementation*. International Journal of Emerging Technology and Advanced Engineering, 3(3):March-2013.

[J4] Sanjay Trivedi, B. S. Raman, **Pinalkumar Engineer** and Dr. Mihir Shah and . *Field Programmable Gate Array Based Control Signal Generator for Pulsed Radar*. International Journal of Embedded Systems and Applications (IJESA), 2(3): September 2012.
https://airccse.org/journal/ijesa/papers/2312ijesa04.pdf

[J3] Rahul V. Shah, Amit Jain, Rutul B. Bhatt, **Pinalkumar Engineer** and Ekata Mehul. *Mean-Shift Algorithm: Verilog HDL Approach*. International Journal of Advanced Research in Computer and Communication Engineering, 1(2):78–85, April 2012.
https://ijarcce.com/wp-content/uploads/2012/05/Mean-Shift-Algorithm-Verilog-HDL-Approach.pdf

[J2] Sanjay Trivedi, B. S. Raman, **Pinalkumar Engineer** and Dr. Mihir Shah. *Design of a Unified Timing Signal Generator (uTSG) for Pulsed Radar*. International Journal of Electronics and Communication Engineering & Technology (IJECET), 3(1): June 2012.
https://iaeme.com/Home/article_id/IJECET_03_01_028

[J1] Dhaval Modi and Harsh Sitapara and Rahul V. Shah and Ekata Mehul and **Pinalkumar Engineer**. *Integrating MATLAB with verification HDLs for functional verification of image and video processing ASIC*. International Journal of Computer Science & Emerging Technologies, 2(2):258–265, 2011.
http://www.ijcset.excelingtech.co.uk/vol2Issue2/09-vol2issue2.pdf

Book Chapters

[B2] Radhika Sreedharan, Jigna Prajapati, **Pinalkumar Engineer**, Deep Prajapati. *Leave-One-Out Validation in Machine Cross-Learning*. In: Ethical Issues in AI for Bioinformatics and Chemoinformatics.
doi:https://doi.org/10.1201/9781003353751

[B1] Jigna Bhupendra Prajapati, Roshani Barad, Meghna B., Kavita Saini, Dhvanil, and **Pinalkumar Engineer**. *Smart Farming Ingredients (IoT Sensors, Software, Connectivity, Data Analytics, Robots, Drones, GIS-GPS)*. In: Applying Drone Technologies and Robotics for Agricultural Sustainability, IGI Publications, 2023.
doi:https://doi.org/10.4018/978-1-6684-6413-7.ch003

Conference Publications

[C21] Hiren Mewada, L. Syam Sundar, **Pinalkumar Engineer**, Miral Desai . *A comparative study between external USB and MIPI CSI for medical imaging and a device driver implementation for endoscope camera using USB*. In: 4th International Conference on Communication,Computing and Industry 6.0 (C2I6-2023).
doi:https://doi.org/10.1109/C2I659362.2023.10430494

[C20] Mitul Sudhirkumar Nagar, Sayantan Maiti, Rahul Kumar, Hiren Mewada, **Pinalkumar Engineer**. *'Memory-efficient Edge-based Non-Neural Face Recognition Algorithm on the Parallel Ultra-Low Power (PULP) Cluster*. In: 16th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC 2023), Singapore University of Technology and Design (STDU), Singapore.
doi:https://doi.org/10.1109/MCSoC60832.2023.00058

[C19] Swati, Ranajoy Sadhukhan, Mitul S Nagar, **Pinalkumar Engineer**. *A Memory Efficient Run-Time Re-Configurable Convolution IP Core for Deep Neural Networks Inference on FPGA Devices*. In: IEEE International Symposium on Smart Electronic Systems (IEEE – iSES), 2023.
doi:https://doi.org/10.1109/iSES58672.2023.00091

[C18] Mitul Sudhirkumar Nagar, Vivek Chauhan, Karnav M. Chinchavde, Swati, Sat Patel, **Pinalkumar Engineer**. *Energy-efficient Acceleration of Deep Learning Based Facial Recognition on RISC-V Processor*. In: International Conference on Intelligent Systems and Embedded Design - (ISED2023).

doi:https://doi.org/10.1109/ISED59382.2023.10444594

[C17] Smita Daware, Shweta Shah, **Pinalkumar Engineer**. *A review on Beamspace Channel Estimation Algorithms in Wireless Communication*. In: 2023 IEEE 7th Conference on Information and Communication Technology (IEEE CICT 2023).
doi:https://doi.org/10.1109/CICT59886.2023.10455367

[C16] Mitul Nagar, Rahul Kumar, **Pinalkumar Engineer**. *Parallelizing Non-Neural ML Algorithm for Edge-based Face Recognition on Parallel Ultra-Low Power (PULP) Cluster*. In: 12th Mediterranean Conference on Embedded Computing (MECO), 2023.
doi:10.1109/MECO58584.2023.10154955

[C15] Swati, Dheeraj Verma, **Pinalkumar Engineer**. *Quantization Effects on a Convolutional Layer of a Deep Neural Network*. In: Congress on Control, Robotics, and Mechatronics (CRM 2023), 2023.
doi:https://doi.org/10.1007/978-981-99-5180-2_32

[C14] Gyaneshwar Rathore, Mitul Nagar, **Pinalkumar Engineer**. *Novel approaches to design 32-bit MAC unit for edge computing devices*. In: National Conference on VLSI and Signal processing and Communication System (NCVSCOMS20), 2020.
https://www.researchgate.net/publication/349210758_Novel_approaches_to_design_32-bit_MAC_unit_for_edge_computing_devices

[C13] Dharmesh Patel, **Pinalkumar Engineer**, Ninad Bhatt. *Image Communication Using Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) Code*. In: International Conference on Advances in VLSI and Embedded Systems, 2019.
doi:https://doi.org/10.1007/978-981-15-6229-7_17

[C12] Syam Sanal, **Pinalkumar Engineer**. *Multithreaded Image Processing Using ReconOS on Reconfigurable Computing System*. In: International Conference on Emerging Trends and Innovations In Engineering And Technological Research (ICETIETR) 2018.
doi:https://doi.org/10.1109/ICETIETR.2018.8529099

[C11] Dharmesh Patel, **Pinalkumar Engineer**. *Design and Implementation of Quasi Cyclic Low Density Parity Check (QC-LDPC) Code on FPGA*. In: International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET 2017), March 22 – 24, 2017. doi:https://doi.org/10.1109/WiSPNET.2017.8299744

[C10] Vinay B. Y. Kumar, **Pinalkumar Engineer**, Mandar Datar, Yatish Turakhia, Saurabh Agarwal, Sanket Diwale and Sachin B. Patkar. *Framework for Application Mapping over Packet-Switched Network of FPGAs: Case Studies*. In: Second International Workshop on FPGAs for Software Programmers (FSP 2015), September 1 – 4, 2015.
doi:https://doi.org/10.48550/arXiv.1508.06823

[C9] Anudeep J, B Chandra Sekhar Naik, and **Pinalkumar J Engineer**. *GPU Implementation of Earth Mover's Distance*. In: 3rd International Conference on Information Technology and Science (ICITS 2015) March 27-30, 2015.

[C8] **Pinalkumar Engineer**, Rajbabu Velmurugan and Sachin B. Patkar. *Parameterizable FPGA Framework for Particle Filter Based Object Tracking in Video*. In: 28th International Conference on VLSI Design, VLSID 2015, Bangalore, India, January 3-7, 2015. pp. 35–40.
doi:https://doi.org/10.1109/VLSID.2015.11

[C7] Sumeet Agrawal, **Pinalkumar Engineer**, Rajbabu Velmurugan and Sachin B. Patkar. *FPGA Implementation of particle filter based object tracking in video*. In: 3rd International Symposium on Electronic System Design (ISED), Kolkata, 19th-22nd December 2012. pp. 82–86.
doi:https://doi.org/10.1109/ISED.2012.41

[C6] Suraj Das, Atit Jariwala and **Pinalkumar Engineer**. *Modified architecture for real-time face detection using FPGA*. In: 3rd Nirma University International Conference on Engineering (Nuicone-2012), Nirma University, Ahmedabad, Dec 6-8,2012. pp. 1–5. doi:https://doi.org/10.1109/NUICONE.2012.6493235

[C5] Suraj Das, Atit Jariwala and **Pinalkumar Engineer**. *FPGA based stream processing of edge and skin detection algorithms*. In: International Conference on Advanced Computing and Communication Technologies (ICACCT-2012) at Asia Pacific Institute of Information Technology SD India, Panipat (Haryana) on November 3,2012.

[C4] Rahul V. Shah, Amit Jain, Rutul B Bhatt, **Pinalkumar Engineer** and Ekata Mehul. *Mean-Shift Algorithm: Verilog HDL Approach*. In: Proceedings of the Third International Conference on Trends in Information, Telecommunication and Computing, 2013. pp 181-194. doi:https://doi.org/10.1007/978-1-4614-3363-7_21

[C3] Dhaval Modi, Harsh Sitapara, Rahul Shah, Ekata Mehul, **Pinalkumar Engineer**. *Combining Power of MATLAB with SystemVerilog for Image and Video Processing ASIC Verification*. In: ADVANCES IN NETWORK SECURITY AND APPLICATIONS, Communications in Computer and Information Science series 2011, 196(1). pp 181-193. doi:https://doi.org/10.1007/978-3-642-22540-6_19

[C2] Dhaval Modi, Harsh Sitapara, Rahul V Shah, Ekata Mehul, **Pinalkumar Engineer**. *Enhancing verification capability using system Verilog and Matlab",*. In: 2nd International conference on Signals, Systems and Automation (ICSSA-2011), January 2011. pp 513-516.

[C1] Hiren Mewada, Pinal K. Patel, **Pinalkumar Engineer**. *FPGA based implementation of computationally efficient Daubchies 9/7 DWT using Lifting scheme*. In: International Conference on Emerging Techniques in Electronics, Computing Embedded System & VLSI Design(ICEVD-2008) at Dr. VV Patil College of Engineering, Ahmednagar, March 20-21, 2008. pp 130.

Conference Posters

[PS1] **Pinalkumar Engineer**, Ayan Mishra, Rajbabu Velmurugan and Sachin B. Patkar. *GPU implementation of Particle Filter based Object Tracking*. In: GPU Technology Conference, GTC 2015, San Jose, California, USA, 2015. Poster abstract.

Industry Interactions

[I6] **aiRender** Industry defined problem for next generation Video conferencing solution

[I5] **TULIPP** Part of TULIPP project (Horizon 2020) during HiPEAC-2019, Valencia, Spain.

[I4] **ARM Ltd.** Donation PSoC 4 Bluetooth® Low Energy (BLE) 4.1 Compliant Pioneer Kits (10 Nos.) for Setting-up Embedded IoT Lab under ARM University program (July 19, 2018).

[I3] **ARM Ltd.** Donation of Keil uVision MDK-ARM version licenses (100 Nos.) for one year (November 23, 2017-November 22, 2018) under ARM University program.

[I2] **Amdocs** One team from SVNIT entered into Top 5 of Grand finale event of *Amdocs Innovation Lab-2017*.

[I1] **Freescale Semiconductor India Pvt. Ltd.** Two teams from SVNIT was a 1st place and 3rd place winners in Grand finale event of *Freescale Cup-2011*.

CONFERENCES/ WORKSHOPS/ STTPS ORGANIZED

[O14] *International Symposium on VLSI Design and Test (VDAT)-2021*. at: ECED, SVNIT Surat, September 16-18, 2021 https://ieeexplore.ieee.org/xpl/conhome/9600867/proceeding

[O13] *TEQIP-III sponsored one week STTP on Recent Trends in Sensors Technology and Automation*. at: ECED, SVNIT Surat & MMMUT Gorakhpur, December 21-25, 2020 https://sites.google.com/eced.svnit.ac.in/sttponsensorsautomation/home

[O12] *International Conference on Advances in VLSI and Embedded Systems (AVES)-2019*. at: ECED, SVNIT Surat, December 20-21, 2019

[O11] *One week workshop on Robotics & IoT*. at: ECED, SVNIT Surat & EICT Academy, MNIT Jaipur, June 17-21, 2019

[O10] *STC on Advanced Analog and Digital VLSI design*. at: ECED, SVNIT Surat, December 26-30, 2017

[O9] *Mentor EDA Tools Training*. at: ECED, SVNIT Surat & SMDP-C2SD, MeiTY, GoI, January 09-12, 2017

[O8] *Two day workshop on Sensor System Design & Automation*. at: ECED, SVNIT Surat, March 11-12, 2016

[O7] *Two day workshop on Embedded Systems in Robotics*. at: ECED, SVNIT Surat, October 9-10, 2015

[O6] *One day Workshop of Wind River Technology Show*. at: ECED, SVNIT Surat, January 19, 2013

[O5] *Two day Workshop on Image Processing*. at: ECED, SVNIT Surat, March 17-18,2012

[O4] *Two day Workshop on Reconfigurable Hardware*. at: ECED, SVNIT Surat, March 17-18,2012

[O3] *Two day Workshop on Virtual DSP Lab*. at: ECED, SVNIT Surat, March 17-18,2012

[O2] *Induction Training Programme*. at: SVNIT, SURAT & EQUATE, January 21-23, 2008

[O1] *Two days workshop on Embedded System Design using PIC Microcontroller*. at: CIT, Changa, March 8-9, 2006

EXPERT LECTURES

[E45] *Selection of Microcontrollers for Drone and Protocols*. at: 5-Days Drone Boot Camp 5.0, March 11, 2024, BMCET (Bhagvan Mahaveer College of Engg. and Technology) and SVNIT Surat.

[E44] *Selection of Microcontrollers for Drone and Protocols*. at: 5-Days Drone Boot Camp 4.0, January 21, 2024, Sarvajanik College of Engineering and SVNIT Surat.

[E43] *A case study/discussion on Digital Circuit/ Reconfigurable FPGA based design*. at: 5-Days Short Term Training Program on Reconfigurable chip design, Image and video analysis using Vivado, LTSpice , Python and OpenCV, May 04, 2023, Parul University, Vadodara.

[E42] *Machine learning and IoT*. at: ONLINE Short-term Training Program (STTP) on Resent Trends in Artificial intelligence and Machine Learning, June 24, 2022, Ramrao Adik Institute of Technology, Nerul

[E41] *M2M IoT Communication Protocols*. at: ATAL FDP on IoT and it's applications, GTU Graduate School of Engineering and Technology, October 4, 2021, GTU Graduate School of Engineering & Technology

[E40] *Embedded processors and operating systems for IoT*. at: R10 HardTec/SofTec summit 2021, IEEE Gujarat Section Chapter, August 25-27, 2021, Sarvajanik College of Engineering & Technology, Surat, August 25, 2021

[E39] *Embedded Computer Vision for Industry 4.0*. at: One-Week Online Short Term Training Program On Research Trends in Control System and Signal Processing (RTCSP -2021), July 5 - 10, 2021, Ramrao Adik Institute of Technology, Navi Mumbai, July 08, 2021

[E38] *Embedded processors and operating systems for IoT*. at: GUJCOST sponsored 3-day workshop on "IoT and Wearable Technology" (8th to 10th April 2021), Sarvajanik College of Engineering, Surat, April 08, 2021

[E37] *Moodle for LMS*. at: STTP on" LMS Enabled Teaching and Learning " during 1-5 December 2020, C.K.P. College of Engg. and Tech., Surat, December 5, 2020

[E36] *Embedded Image processing using FPGA*. at: AICTE sponsored short term technical training programs (STTP) on "FPGA Design and Implementation on Xilinx Tools", ABES Engineering College, Ghaziabad, September 25, 2020

[E35] *VLSI Signal Processing*. at: AICTE sponsored Six Days Online FDP On Advanced VLSI Design and Applications with hands-on CADENCE Tools(Digital ASIC Design using CADENCE EDA Tools), ABES Engineering College, Ghaziabad, August 29, 2020

[E34] *Moodle LMS*. at: Online Programme on ICT Tools for Teaching, Learning Process & Institutes, MNIT Jaipur, August 17, 2020

[E33] *Real-time system design using Embedded Microcontrollers*. at: Online Webinar, GEC, Surat, June 05, 2020

[E32] *Designing a 3D printer*. at: ATAL Academy workshop on "Reverse Engineering", MED, SVNIT Surat, January 10, 2020

[E31] *Design of Microprocessor for IoT Applications*. at: FDP on Recent trends in Internet of Things (IoT), St. John College of Engineering and Management, Palghar, June 14, 2019

[E30] *Hands on Session of IoT using Bluetooth LE*. at: FDP on Recent trends in Internet of Things (IoT), St. John College of Engineering and Management, Palghar, June 14, 2019

[E29] *Vivado design flow for Advanced FPGA Design*. at: One week FDP on Digital VLSI Systems Design and Implementation, MNIT Jaipur

[E28] *Inkscape for Document writing*. at: STTP on Paper and Article Writing with LaTeX, SVNIT, Surat, January 18, 2018

[E27] *Reconfigurable Computing*. at: One Week Short Term Course on Advanced Analog and Digital VLSI Design, SVNIT, Surat, December 30, 2017

[E26] *CPLDS*. at: One Week Short Term Course on Advanced Analog and Digital VLSI Design, SVNIT, Surat, December 30, 2017

[E25] *IP integration*. at: One Week Academy Training Programme on CAD Tools for Advanced Digital Design using FPGAs, MNIT Jaipur, December 12, 2017

[E24] *RTL Synthesis*. at: One Week Academy Training Programme on CAD Tools for Advanced Digital Design using FPGAs, MNIT Jaipur, December 12, 2017

[E23] *Implementation using Vivado*. at: One Week Academy Training Programme on CAD Tools for Advanced Digital Design using FPGAs, MNIT Jaipur, December 11, 2017

[E22] *Introduction to Robotics*. at: Essar Technology Day, Essar Ltd, Hazira, September 13, 2017

[E21] *Inkscape*. in: STTP on Paper and Article Writing with LaTeX at Electronics Engineering Department, S V National Institute of Technology, Surat, January 24, 2017.

[E20] *Introduction to Parallel Computing*. in: One day Training under Industry defined research project under Newton-Bhabha Fund at Parul University, Vadodara, March 15, 2017.

[E19] *Introduction to Linux*. at: Electronics Engineering Department, Government College of Engineering, Valsad, October 15, 2016.

[E18] *Hardware/Software co-design for Embedded System design*. at: Electronics Engineering Department, Dr. S. S. Gandhi Government College of Engineering, Surat, September 29, 2016.

[E17] *Image processing using GPU*. in: STTP on Emerging Trends in Signal & Image Processing (ETSiP) at Electronics Engineering Department, S V National Institute of Technology, Surat, September 17, 2016.

[E16] *FreeRTOS*. at: V. T. Patel Department of Electronics and Communication Engineering, Chandubhai S Patel Institute of Technology (CSPIT) Charotar University of Science and Technology (CHARUSAT) - Changa, February 13, 2015.

[E15] *Embedded Image processing using FPGAs*. at:GUJCOST Sponsored workshop on Software and Hardware Realization for Image & Video Processing and its Applications. V. T. Patel Department of Electronics and Communication Engineering, Chandubhai S Patel Institute of Technology (CSPIT) Charotar University of Science and Technology (CHARUSAT) - Changa. January 29, 2015.

[E14] *Real-time Image processing using OpenCV and GPU*. at: GUJCOST Sponsored workshop on Software and Hardware Realization for Image & Video Processing and its Applications. V. T. Patel Department of Electronics and Communication Engineering, Chandubhai S Patel Institute of Technology (CSPIT) Charotar University of Science and Technology (CHARUSAT) - Changa. January 29, 2015.

[E13] *Multithreading Programming using pThreads and CUDA*. at: TEQIP-II sponsored Workshop on High Performance Computing-Architectures and applications for Engineer and Scientists. SVNIT, Surat. January 25, 2015.

[E12] *Hardware & Software co-design for secure embedded systems*. at: C K Pithawala College of Engineering & Technology, Surat. August 30, 2015.

[E11] *Embedded System Design Methodology*. at: Mindbend. SVNIT, Surat. October 25, 2013.

[E10] *ARM processor Pin Functioning and Instruction Set*. at: STTP on Embedded System Design using Assembly and C Language. Institute of Diploma Studies, Nirma University. May 30, 2012.

[E9] *Introduction to PIC Microcontrollers*. at: STTP on Embedded System Design using Assembly and C Language. Institute of Diploma Studies, Nirma University. May 29, 2012.

[E8] *Design, Implementation & Modeling of Mixed Design Embedded Systems*. at: STTP on Advanced on Embedded Systems. RK University, Rajkot. December 20, 2011.

[E7] *Structural Modelling*. at: SMDP II Sponsored ISF Organised two day workshop on VHDL. ECED, SVNIT, SURAT. September 19, 2010.

[E6] *Use of Analog and Digital Oscilloscopes*. at: ISF(IETE), SVNIT. November 21, 2009.

[E5] *Hardware Description Languages*. at: National Workshop on VLSI Design tools sponsored by SMDP-II Project. ECED, SVNIT, SURAT. February 28- March 1, 2009.

[E4] *Introduction to HDL*. at: Faculty Development Program sponsored by TEQIP. ECED, SVNIT, SURAT. December 15-19, 2008.

[E3] *ARM 7 Core*. at: STTP on Embedded System:Approach, Applications & Design. PIET, Vaghodia. July 09, 2008.

[E2] *ARM Processors-Why ARM & Various Families*. at: STTP on Embedded System:Approach, Applications & Design. PIET, Vaghodia. July 09, 2008.

[E1] *ARM 7 Instruction Set*. at: STTP on Embedded System:Approach, Applications & Design. PIET, Vaghodia. July 09, 2008.

PROFESSIONAL SERVICE

Conference Service

- Publicity chair: 9th IEEE International Symposium on Smart Electronic Systems (iSES) – 2023. December 18-20, 2023
- Publication chair: VLSI Design Conference (VLSID)-2022. February 26-March 2, 2022
- General chair: International Symposium on VLSI Design and Test (VDAT)-2021. September 16-18, 2021
- Local Organizing Committee: 3^{rd} International Conference on Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2020. February 7-8, 2020
- Organizing chair: 1^{st} International Conference on Advances in VLSI and Embedded Systems (AVES)-2019. December 20-21, 2019
- Local Organizing Committee: EAI International Conference on FUTURE INTERNET TECHNOLOGIES AND TRENDS, 2017. August 31 - September 2, 2017
- Local Organizing Committee: 2^{nd} International Conference on Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2014. December 26-27, 2014
- Local Organizing Committee: 1^{st} International Conference on Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2012. December 19-21, 2012

PROFESSIONAL MEMBERSHIPS

- Institute of Electrical and Electronics Engineers (IEEE) (2009–present)
- The Institution of Electronics and Telecommunication Engineers (IETE) (2002–present)
- RISC-V International (2020–present)
- Association for Computing Machinery (ACM) (2021-present)