25th International Symposium on VLSI Design and Test (VDAT-2021)

Sardar Vallabhbhai National Institute of Technology Surat, India

September 16-18, 2021

www.vlsidat.org

VLSI Society of India

Call for Papers

Theme: Intelligent Systems for Humanity

About VDAT

VDAT began as a small workshop in the year 1998. In 2005, it acquired the status of a Symposium. The purpose of the Symposium is to promote the advancement of all aspects of VLSI. The 25th International Symposium on VLSI Design and Test (VDAT-2021) is to be held at Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat, India. The aim of this symposium is to bring academics, researchers, startups and industrial practitioners together to exchange their ideas in the area of VLSI design, test and system design.

Tracks

Researchers, academicians and professionals are invited to submit papers in the following topics (but not limited to)

Devices Modeling and Emerging Devices/Material Technologies

MOS Device Modeling and Simulation; Multi-gate and other Emerging MOS devices. Si-Photonics and Optoelectronics devices; MEMS/NEMS; Organic electronics; 2D and advanced material-based electronics; Flash memory devices and other emerging memory technologies like ReRAM, PCM, SSTRAM etc.

VLSI Circuit and System Design

Low power, High-performance and robust design of logic, memory, analog, RF and FPGA based circuits; Clock-generation and distribution circuits including all-digital PLLs and DLLs; ADC's and DAC's; Soft-error and fault-tolerant circuits; Circuit design for reliability effects such as gate oxide integrity, electro-migration, ESD, HCI, NBTI, PBTI etc.; On-chip process, voltage, temperature, and aging sensors and monitoring systems; Hardware accelerators for machine learning (ML) and deep learning algorithms; Hardware implementations of ML algorithms for applications like image/object recognition, computer vision, speech recognition, and natural language processing; ML-based intelligence in IoT under highly constrained design requirements; Secure and intelligent system on chip (SoC) design for automotive, health, defense applications etc.

CAD for VLSI and Hardware Security

Logic and behavioral synthesis; Placement, Routing and Floor planning; CAD tools; Design automation; Hardware attack detection; Threat modeling & defense; Hardware-based security primitive design; Trusted design automation, Tools & Information flow.

Testing and Verification

Design verification, Test, Reliability and Fault tolerance; Formal verification; DFT; Fault modeling; Post-silicon validation; Testing memories and regular logic arrays; Design for manufacturability and yield analysis.

FPGA based Design and Embedded Systems

FPGA based combinational/sequential logic/circuit design, Hardware/Software co-design and verification; Audio, Image and video processing; Reconfigurable systems; Microcontroller, IoT and FPGA based embedded systems design; Embedded software; CAD for embedded systems; Artificial intelligence and ML based systems.

Soft copies of papers should be submitted in .pdf format as per the IEEE conference paper format not exceeding six A4 size pages and paper should be uploaded through online portal. There will be double blind review of the paper. Therefore, do not include authors' name in submitted paper. A paper with authors' details will not be considered for review.

Important dates:

Regular Papers:
- Full Paper Submission: ~~June 10, 2021~~ ~~June 24, 2021~~ **July 03, 2021**
- Notification of Acceptance: **August 16, 2021**
- Camera Ready Paper: **August 26, 2021**

Tutorials:
- Tutorial Proposal Submission: **June 30, 2021**
- Tutorial Date: **September 16, 2021**

Conference: September 17 - 18, 2021

Takeaway

Tutorial:
Tutorials are invited on the cutting-edge research and technology in the area of advanced materials/devices, circuit and systems.

Design Contest:
The contest has two divisions. One is to design the analog/ digital/RF/ mixed signal module using EDA tools and other one is to design and demonstrate the safe and secure intelligent systems using hardware. The forum will provide opportunities to the participants to learn hands on practice for chip to system design (C2SD) and embedded system design using sensors and advanced interface devices.

Fellowship (Registration):
The fellowship covers the registration cost. To avail the fellowship, please keep eye on symposium site.

Forums

Student Research Forum:
Students, including bachelors, masters and PhDs may participate in this forum through presenting their work for better technical inputs to further improve the quality of work. This forum may also provide an opportunity to the students to establish the network with industry players for job perspective.

Women in Engineering Forum:
The forum will provide the opportunities to the female participants for accelerating their engagement in the area of VLSI chip design, testing and embedded systems.

Submission Instructions

All papers must be submitted through the CMT at:
https://cmt3.research.microsoft.com/VDAT2021

For more details:
www.vlsidat.org

Email: vdat2021@gmail.com