



Name: Anand D. Darji

Date of Joining: 1st August, 2000

Highest Qualification: M.Tech (Electronic Systems), **IIT Bombay (CPI 9.02)**

Designation: Assistant Professor

Research Interest: VLSI Design, Embedded System Design, Electronics Instrumentation, Signal Processing

Research Publications:

a) International Journals

1. Taral D. Chhatbar, Anand Darji ,”FPGA Implementation of 2048-Point FFT/IFFT High speed Architecture, ”International Journal of emerging Technologies in Engineering Technology and Sciences,Vol.2,No.2 ,pp.785-788,2009
2. Amit Joshi, Anand Darji,” Secure Digital Camera With DWT based Watermarking,” ”International Journal of emerging Technologies in Engineering Technology and Sciences,Vol.2,No.2 ,pp.813-818,2009

b) International Conferences

1. Hiren mewada and Anand Darji , ”Reconfigurable Implementation of New Millennium Standard JPEG 2000”, IEEE Indicon 2007, International Conference on Advanced Electrical, Electronics, Communication and Information Technology , Central Power Research Institute (CPRI) Bangalore Date: 6-8 Sept 2007
2. Joshi Ketki, Darji A.D., Dalal U.D, “Design and Analysis of Low power VITERBI Decoder For CDMA Communication System,” 13th IEEE/ VSI VLSI Design And Test Symposium (VDAT-2009), IEEE/VLSI Society of India, Wipro Campus, Electronic City, Bangalore, pp.358-369, 8-10 July 2009
3. Joshi A.M, Darji A.D.,” Efficient Dual Domain Watermarking Scheme for Secure Images,” International Conference on Advances in Recent Technologies in Communication and Computing, 2009. (ARTCom '09), Kottayam, Kerala, pp.909-914,27-28 Oct, 2009
4. Chhatbr T.D., Darji A.D.,” High Speed High Throughput FFT/IFFT Processor ASIC for Mobile Wi-Max,” Second International Conference on Emerging Trends in Engineering and Technology (ICETET-09), IEEE Systems, Man & Cybernetics Society and C.H.Raisoni College of Engineering, Nagpur,pp.402-405, 16-18 Dec 2009

c) National Conferences

1. Anand Darji and Hiren mewada , ”Recent Trend in Data Compression using Wavelet” , National Conference on Engineering Trend in Electronics (NCETE) at MAE Pune, pp.221-226, 28-29 Dec,2006

2. Taral Chhatbar and Anand Darji, "A Comparative Study of FFT Algorithms and Implementation on FPGA" Emerging Trends in Communication & Computing (ETCC) at NIT, Hamirpur, 27-28 July, 2007
3. Amit M Joshi, Anand Darji, Taral D Chhatbar, Abhishek Aghrahari, "Clock skew analysis and optimization of sequential circuit", NCIS 07, M.J. College of Engineering and Technology, Hyderabad, 24-25 August, 2007
4. Vipul Mistry, Anand Darji, "Hardware implementation of DWT/IDWT Processor", Indian conference on Computer vision, Graphics, Image and Video Processing, R.K. Nehru Engineering College, Nagpur, March 13-14, 2009

Research Grant/Project

1. Modernization of Digital Signal Processing Lab, Funding Agency MHRD, Project Duration : 2Year, 4.5 Lacs
2. Special Manpower Development Project for VLSI Design and Related Software , Project Duration 5 Years, 1 Crore

Consultancy Report:

Anand Darji and S.C. Patwardhan; "Performance Analysis of Zigbee (IEEE 802.15.4) enabled wireless sensor network for Control Applications"; Consultancy Report for Honeywell Technological Solution Limited, Bangalore; 2006 (Research Work done at Automation Lab, IIT Bombay)

M Tech Dissertation Supervision (Completed):

1. Reconfigurable Implementation of New Millennium Standard – JPEG 2000, Hiren Mewada, 2006-07
2. Poly phase Filter bank Implementation using FPGA, Nagendra Prasad, 2007-08
3. FPGA Implementation of MDCT/IMDCT for Audio Codec Application, Niraj Gupta, 2007-08
4. VLSI Implementation of DWT based watermark Embedding Hardware for Digital Camera, Vipul Mistry, 2008-09
5. VLSI Design of Low Power Viterbi Decoder For CDMA Communication Systems, Ketki Joshi, 2008-09
6. FPGA Implementation of Watermarking Algorithm for Digital camera, Amit Joshi, 2008-09
7. SOC Level Verification using System Verilog, Purvi Mulani, 2008-09
8. 2048 Point FFT/IFFT Implementation for Mobile Wi-Max System, Taral , 2008-09

On Going M.Tech Projects:

1. Low power Area efficient Pipelined FFT/IFFT Processor Design using 180 nm Standard Cells, Manish Patil

Expert Lecturers

1. "Interfacing I/O" at Udbhav-2007 CKPCET, Surat (Dt: 23/2/2007)
2. "Wireless sensor Network " at STTP – Recent trend in embedded systems", SCET, Surat (Dt: 20/12/2006)
3. "ZIGBEE: Wireless sensor network for Automation" at STTP Advanced control system at DDIT, Nadiad.
4. " Embedded System Development Cycle: A case study of 3- phase heater controller" , ISTE-STTP on VLSI and Embedded Systems: Design and Applications, SCET ,Surat Dt 11/5/2008
5. "Embedded Software Architecture" , ISTE-STTP on VLSI and Embedded Systems: Design and Applications, SCET ,Surat Dt 13/5/2008
6. " Embedded System Development Cycle : A Case study on 3-Phase Heater Controller, ISTE-STTP on VLSI and Embedded Systems: Design and Applications, SCET ,Surat , 9-14 May, 2008

7. "Hard ware Description language" at Mindbend 2007, SVNIT
8. "SPICE and Magic CAD tool", Faculty Development Program sponsored by TEQIP , SVNIT,15-19 Dec 2008
9. "LIFE with SPICE", National Workshop on VLSI Design tools sponsored by SMDP-II Project ,Department of Information Technology (DIT), New Delhi, SVNIT, Feb 28- March 1 , 2009
10. "Integrated circuit (IC) Design flow," National Workshop on VLSI Design tools sponsored by SMDP-II Project ,Department of Information Technology (DIT), New Delhi, SVNIT, Feb 28- March 1 , 2009
11. "ADC Architectures," AICET Sponsored National Level Short Term Training Program on Microcontrollers and Their Applications, SVNIT, 14-18 Dec. 2009
12. "MATLAB for Semicustom Chip Design," AICET Sponsored National Level Winter School, Teaching with MATLAB and Simulink ,SVNIT, 21-25 Dec 2009

STTPs/Conferences Organized:

National Workshop on VLSI Design tools, 28 Feb-1 March, 2009, SVNIT Surat.

STTPs/Conferences Attended:

1. Workshop on Low Power VLSI Design, Nirma University, 29-30 Jan ,2010
2. Instruction Enhancement Program (IEP) on Mixed Signal VLSI Design, IIT Bombay, 16-21 March, 2009
3. National Workshop on PhD Research in VLSI,DA-IICT, Gandhinagar, 11 Jan 2009
4. Advanced engineering optimization through intelligent Techniques, SVNIT-ISTE, 30 June-4 July, 2008
5. Management Capacity Development for Middle level faculty (Future Manager), SVNIT-TEQIP, SVNIT, 4 -8 Feb, 2008
6. Embedded Linux on ARM, SPJ Embedded Tech, PUNE 18-20 Oct., 2007
7. Analog IC Design, IITD Delhi, 03- 14 July, 2007
8. Xilinx Workshop on Embedded Systems, Xilinx & IITB, 09-10 March, 2007
9. National Workshop on Challenges in VLSI (NWCV-2006) DAIICT, Gandhinagar, 21-22 Dec, 2006
10. TI Developer Conference, TIDC-2006, Texas Instrument 30 Nov -1 Dec, 2006
11. Multi core Workshop, INTEL & IIT Madras 11 Nov, 2006
12. MATLAB For analysis and simulation of Electrical, Electronics and Control systems, ISTE & NIRMA UNIVERSITY 01-12 Dec., 2003
13. Advance Communication Systems AICTE/ISTE & SVNIT,SURAT 24-29 Dec.,2001
14. VLSI System Design ISTE & REC WARANGAL 23 July - 4 Aug., 2001

Administrative Responsibilities:

Current: Co-coordinator SMDP-II Project of Govt. of India to generate trained manpower in the field of VLSI Design and related CAD tools, Convocation committee member, Lab In charge of Electronics System Design Lab and VLSI Design Lab, MIS Committee Member

Past: Co convener of Mindbend-2008, Faculty Advisor of IETE Student chapter, Co-coordinator of Modernization of Digital Signal Processing Lab Project, Reviewer of International/National Conferences and Journals. Review VLSI Design book (Oxford Publications)

Other Information:

I am perusing Ph.D. in the field of VLSI Design from IIT Bombay under Prof. A.N. Chandorkar and Prof. S.N.Merchant. We have design chip for 2048 Point FFT/IFFT processor using UMC 180 nm technology under SMDP-II project. I am life member of ISTE Society. I have guided 30 B.Tech Project and 45 B.Tech Seminar